OPTIMIZED TECHNOLOGY MAPPING TECHNIQUES FOR PROGRAMMABLE CIRCUITS

ABSTRACT OF THE DISCLOSURE

[0117] Technology mapping techniques are provided for converting a user design for a programmable integrated circuit to a network of programmable logic blocks. The technology mapping process attempts to combine each non-strategic node and predecessor nodes in one programmable logic block according to only one type of node merging group. If the non-strategic node can be feasibly merged with predecessor nodes according to the merging group, they are grouped into a programmable logic block. The technology mapping process tries to merge strategic nodes with various merging groups of predecessor nodes to form a programmable logic block. The technology mapping process can select the best merging group for the strategic node by using a cost metric. The cost metric can consist of depth and area information of a network for the logic cone.